a gate electrode formed only on said first side of the silicon layer between the first diffused region and the second diffused region interposing a gate insulating film between the gate electrode and the silicon layer;

a contact electrode formed on said first side of the silicon layer and connected to the second diffused region; and

a capacitor formed only on said first side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said second side of the silicon layer and electrically connected to the second diffused region via the contact electrode;

a support substrate formed on said first side of the silicon layer for supporting the device layer interposing an insulating film between the support substrate and the device layer; and

a strapping word line formed on said second side of the silicon layer and connected to the gate electrode.

30. (New) A semiconductor memory device comprising:

a device layer including:

a silicon layer having a first diffused region and a second diffused region formed therein and having substantially flat surfaces, said silicon layer defining a first side and a second side;

a gate electrode formed only on said first side of the silicon layer between the first diffused region and the second diffused region interposing a gate insulating film between the gate electrode and the silicon layer;

a contact electrode formed on said first side of the silicon layer and connected to the second diffused region; and

a capacitor formed only on said first side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said second side of the silicon layer and electrically connected to the second diffused region via the contact electrode;

a support substrate formed on said first side of the silicon layer for supporting the device layer interposing an insulating film between the support substrate and the device layer; and

a strapping word line formed on said first side of the silicon layer and connected to the gate electrode.

31. (New) A semiconductor memory device comprising:

a device layer including:

a silicon layer having a first diffused region and a second diffused region formed therein and having substantially flat surfaces, said silicon layer defining a first side and a second side;

a gate electrode formed only on said first side of the silicon layer between the first diffused region and the second diffused region interposing a gate insulating film between the gate electrode and the silicon layer;

a contact electrode formed on said first side of the silicon layer and connected to the second diffused region; and

a capacitor formed only on said first side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said second side of the silicon layer and electrically connected to the second diffused region via the contact electrode;

a support substrate formed on said first side of the silicon layer for supporting the device layer interposing an insulating film between the support substrate and the device layer; and

a shield electrode formed above the bit line for suppressing interference between the bit lines.